Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (Previously Presented) The power amplifier according to claim 6 wherein said active element comprises a VLSI CMOS transistor.

3. (Previously Presented) The power amplifier according to claim 6 wherein said active element comprises a high frequency bipolar transistor.

4. (Original) The power amplifier according to claim 2 wherein said DMOS transistor is sized and biased so that the VLSI CMOS transistor works in saturation area and complies with a relation:

$$Vx \geq (Vg2 - V_{th2})$$

wherein:

Vx is a voltage value on a terminal of said VLSI CMOS transistor;

Vg2 is a voltage value on a control terminal of said VLSI CMOS transistor; and

Vth2 is a threshold voltage value of said VLSI CMOS transistor.

5. (Previously Presented) The power amplifier according to claim 6 wherein said load element has a control terminal to receive a first control voltage being set so that the active element works in a saturation area.

6. (Currently Amended) A power amplifier, comprising:

at least a load element and at least an active element inserted, in series to each other, between first and second voltage references, wherein said load element includes a DMOS transistor; and

a resistive element, inserted between a circuit node connecting said active element to said load element and said second voltage reference, to stabilize the circuit node.

7. (Canceled)

8. (Previously Presented) The apparatus of claim 11 wherein the load element comprises a DMOS transistor.

9. (Previously Presented) The apparatus of claim 11 wherein the active element comprises a VLSI CMOS transistor.

10. (Previously Presented) The apparatus of claim 11 wherein the active element comprises a bipolar transistor.

11. (Previously Presented) An apparatus, comprising:

a load element having a first terminal coupled to a first voltage reference, a second terminal coupled to receive a first control voltage, and a third terminal coupled to a node; and

an active element in cascode configuration and having a first terminal coupled to the third terminal of the load element at the node, a second terminal coupled to receive a second control voltage, and a third terminal coupled to a second voltage reference; and

a resistive element coupled between the first and third terminals of the active element to stabilize the node at the first terminal of the active element,

wherein the second control voltage is set and integration limits of the load element are fixed to allow the active element to operate in a saturation area to provide high cutoff frequency and a high transconductance value and in a linear area to prove low activation resistance.

12. (Previously Presented) The apparatus of claim 11 wherein the load element and the active element are coupled to provide a high breakdown voltage in the saturation area.

13. (Canceled)

14. (Previously Presented) The power amplifier of claim 17 wherein the transistor load element and the active element are coupled to provide a high breakdown voltage in the saturation area.

15. (Previously Presented) The power amplifier of claim 17 wherein the transistor load element comprises a DMOS transistor.

16. (Previously Presented) The power amplifier of claim 17 wherein the active element comprises either a VLSI CMOS transistor or a bipolar transistor.

17. (Currently Amended) A power amplifier usable in radio frequency applications, the power amplifier comprising:

first and second voltage references;

a transistor load element having a first terminal coupled to the first voltage reference, a second terminal coupled to receive a first control voltage, and a third terminal coupled to a node;

an active element in cascode configuration and having a first terminal coupled to the third terminal of the transistor load element at the node, a second terminal coupled to a second control voltage, and a third terminal coupled to the second voltage reference, wherein the transistor load element is sized and biased and the second control voltage is set to allow the active element to operate in a saturation area to provide high cutoff frequency and a high transconductance value and in a linear area to prove low activation resistance; and

a resistive element to stabilize the node and coupled between the first and third terminals of the active element in a manner that a first terminal of the resistive element is coupled to the node and a second terminal of the resistive element is coupled to the second voltage reference.

18. (Canceled)

19. (Previously Presented) A method, comprising:

sizing and biasing a transistor load element to allow an active element to operate in a saturation area;

receiving a first control voltage at a control terminal of the load element to allow the active element to operate in the saturation area;

setting a second control voltage at a control terminal of the active element to allow the active element to operate in the saturation area; and

obtaining high cutoff frequencies and high transconductance values in the saturation area, and obtaining low on-state resistance values in a linear area of operation; and

stabilizing a circuit node between the transistor load element and the active element with a resistive element having a first terminal coupled to the circuit node and a second terminal coupled to a voltage reference.

20. (Previously Presented) The method of claim 19, further comprising obtaining high breakdown voltage values in the saturation area.

21. (Canceled)

22. (Previously Presented) The apparatus of claim 23, further comprising a means for obtaining high breakdown voltage values in the saturation area.

23. (Previously Presented) An apparatus, comprising:

means for sizing and biasing a transistor load element to allow an active element to operate in a saturation area;

means for receiving a first control voltage at a control terminal of the load element to allow the active element to operate in the saturation area;

means for setting a second control voltage at a control terminal of the active element to allow the active element to operate in the saturation area; and

means for obtaining high cutoff frequencies and high transconductance values in the saturation area, and for obtaining low on-state resistance values in a linear area of operation; and

means for stabilizing a circuit node between the transistor load element and the active element, the means for stabilizing being coupled between a pair of terminals of the active element that are different from the control terminal of the active element.

24. (Previously Presented) The apparatus of claim 23 wherein the means for stabilizing the circuit node comprises a resistive element.